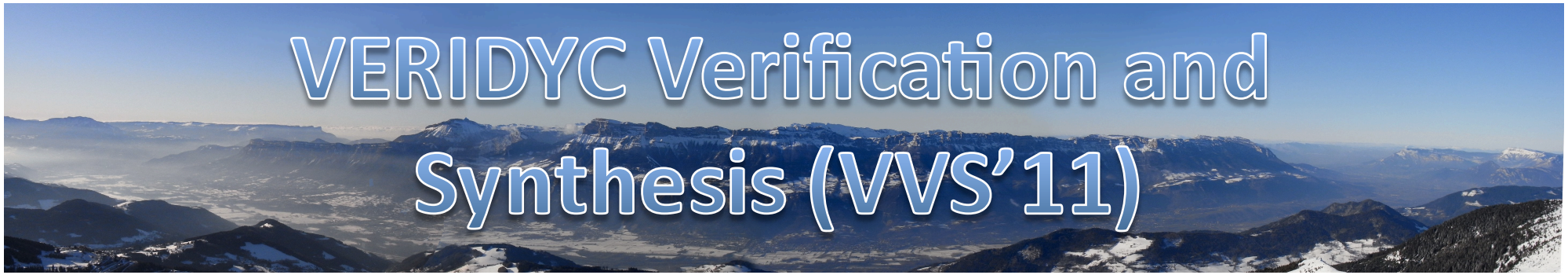

VERIDYC Verification and Synthesis (VVS'11)

June 30th, 2011, Verimag (CTL), Grenoble

9h00 *Welcome and coffee*

9h30 Ahmed Bouajjani (LIAFA) *Verifying concurrent programs running over TSO*

10h30 Coffee break

11h00 Ruzica Piskac (EPFL) *Software Synthesis using Automated Reasoning*
11h30 Barbara Jobstmann (VERIMAG) *Quantitative Verification and Synthesis*
12h00 Nicolas Halbwachs (VERIMAG) *Static Analysis of Programs with Arrays*
12h30 Cezara Dragoi (LIAFA) *On Inter-Procedural Analysis of Programs with Lists and Data*

13h00 *On-site lunch break*

14h00 **VERIMAG seminar:** Nathalie Bertrand (IRISA) *Determinizing timed automata*

15h00 Pierre Corbineau (VERIMAG) *On Positivstellensatz Witnesses in Degenerate Cases*
15h30 Michael Emmi (LIAFA) *On Sequentializing Concurrent Programs*
16h00 Jules Villard (LSV/Queen Mary) *Tracking Heaps that Hop with Heap-Hop*

16h30 *Coffee break*

17h00 VERIDYC business meeting

Register for free at **http://www-verimag.imag.fr/VVS.html**

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